REMARKS

In response to the Office Action mailed October 2, 2003, Applicant respectfully requests reconsideration. To further the prosecution of this Application, Applicant submits the following remarks, has amended a claim and has added new claims. The claims as now presented are believed to be in allowable condition.

Claims 1-32 were pending in this Application. By this Amendment, claims 33-42 have been added. Accordingly, claims 1-42 are now pending in this Application. Claims 1, 11, 21, 30 and 31 are independent claims.

Preliminary Matters

Applicant wishes to thank Examiner Bragdon for the clear and detailed explanations provided in the Office Action. Such clarity and detail was extremely helpful in enabling Applicant to select and provide an effective response strategy to further the prosecution of this Application.

Rejection under §112, First Paragraph

Claim 20 was rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement. In particular, the Office Action contended that, in claim 20, it is not clear where Applicant has set forth a status message that includes a non-reserved value as a tag indicator when a data element is valid and a reserved value as the tag indicator when the data is invalid (see paragraph 3 of the Office Action).

Applicant has made a clarifying amendment to claim 20 to cure this informality. As a result, Applicant respectfully submits that the Specification contains a clear description of the invention as recited in claim 20, as amended. For example, a clear description is provided on page 20, lines 15-21 of the Specification. Accordingly, the rejection of claim 20 under 35 U.S.C. §112, first paragraph, should now be withdrawn.

Rejections under §102 and §103

Claims 1-4, 11-14, 21-24 and 30-31 were rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,389,494 (Walton et al.) which incorporates by reference U.S. Patent No. 6,145,042 (Walton). Claims 1, 11, 21 and 30-31 were further rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,578,108 (Fujimoto et al.). Claims 1-31 were rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,425,034 (Steinmetz et al.).

Applicant respectfully traverses each of these rejections and requests reconsideration. The claims are in allowable condition because they patentably distinguish over each of the cited references as will now be explained.

Walton '494 discloses a computer system 100 which includes an interface 100 having a cache memory section 120 and eight directors 122_0-122_7 (column 3, lines 38-58 and Fig. 2). The interface 118 includes a plurality of serial end-user data busses $126_{0,0}$-$126_{7,1}$ for carrying end-user data (column 4, lines 23-25 and Fig. 2). Each one of the plurality of end-user data busses $126_{0,0}$-$126_{7,1}$ has a first end coupled to a corresponding one of the plurality of directors 122_0-122_7, and a second end couple to the memory section 120 (column 4, lines 25-30 and Fig. 2). The interface 118 also includes an interface state data bus section 124 made up of four interface state data parallel (72 wire) busses, i.e., bus A, bus B, bus C and bus D, for carrying interface state data through the interface 118 (column 4, lines 15-19 and Fig. 2). In the cache memory 120, end-user data is selectively coupled through a coupling node 130 in accordance with routing information fed thereto by ASICs A,A through D,D (column 5, lines 41-44 and Fig. 3). Each one of the ASICs A,A through D,D is identical in construction (ASIC A,A being an exemplary one) and includes control logic 150 and buffer memory 152 which are further described in Walton '042, which is referred to in Walton '494 as Ser. No. 08/996,809 (column 5, lines 56-66 and Fig. 6). The control logic 150 includes a decoder 157 for decoding eight chip select signals and one read/write signal on the A bus (column 6, lines 21-27 and Fig. 6).

Walton '042 discloses an interface 18 having controllers 20, 22, addressable cache memories 24a, 24b, 24c, 24d, and buses 26, 28 (column 4, line 60 through column 5, line 5 and Fig. 1B). Each bus 26, 28 has bus-select/address/command portion 28a, a bus-grant/data/clock-pulse/queue portion 28b and an ending-status portion 28c (column 6, lines 10-14 and Fig. 2). Each controller 20, 22 is adapted to assert a command on the bus portion 28a such as a read or write operation request, and to produce data and clock pulses on the portion 28b (column 6, lines 14-29). Similarly, each of the addressable cache memories 24a, 24b, 24c, 24d is adapted to produce a bus grant signal and to provide data on the portion 28b (column 6, lines 30-58).

Fujimoto discloses a disk array controller 1 having selector units 13, cache memory units 14, and CM access controllers 104 for controlling access to the cache memory units 14 (column 6, lines 24-55 and Fig. 1). Each cache memory unit 14 includes a memory module 106 and a CM controller 114 (column 7, lines 6-10 and Fig. 6). The CM controller 114 moves data into and out of the memory module 106 through an access path 136 in accordance with signals (REQ, ACK, etc.) through control lines 213 (column 9, line 21 through column 11, line 26).

Steinmetz discloses a host bus adaptor 182 which connects to a number of peripheral devices 186 through a high-speed serial FC data stream 188 (column 8, lines 45-54 and Figs. 4 and 5). The host bus adaptor 182 utilizes a fibre channel controller 190 (column 8, lines 55-58). Steinmetz further discloses a disk array controller 200 which uses the fibre channel controller 190 (column 8, lines 64-65 and Figs. 5 and 6). In particular, the disk array controller 200 includes a cache memory 210 which connects to a first FC controller 206 through a first PCI bus 208, and connects to more FC controllers 216A-216N through a second PCI bus 214 which interface to a mass storage system 204 (column 9, lines 1-8 and Fig. 6).

Claims 1-10

Claim 1 is directed to a method for exchanging data with a volatile memory cache circuit. The method is performed in an interface circuit of a data storage system. The method includes the steps of providing a command to the volatile memory cache circuit through a point-to-point channel between the interface circuit and the volatile memory cache circuit, moving a data element through the point-to-point channel in accordance with the command, and receiving status from the volatile memory cache circuit through the point-to-point channel in accordance with the data element.

The cited references do not teach such a method as will now be explained. Since claim 1 was individually rejected under 35 U.S.C. §102(e) by Walton '494, Fujimoto and Steinmetz, Applicant will address each reference individually.

First, Walton '494 does not disclose a method having a step of providing a command a volatile memory cache circuit through a point-to-point channel between the interface circuit and the volatile memory cache circuit, as recited in claim 1. Rather, Walton '494 discloses an interface 118 having an interface state data bus section 124 made up of four interface state data parallel (72 wire) busses, i.e., bus A, bus B, bus C and bus D, for carrying interface state data through the interface 118 (see column 4, lines 15-19 and Fig. 2 of Walton '494). Walton '494 clearly and unambiguously explains that a coupling node 130 of the cache memory 120 selectively couples end-user data therethrough in accordance with routing information fed thereto by ASICs A,A through D,D (see column 5, lines 41-44 and Fig. 3 of Walton '494). In particular, each ASIC has control logic 150 including a decoder 157 for decoding eight chip select signals and one read/write signal on a bus (e.g., the A bus) (see column 6, lines 21-27 and Fig. 6 of Walton '494). Accordingly, if one were to argue that the routing information of Walton '494 are commands, those commands pass through the busses A, B, C, and D not a point-to-point channel.

In support of the rejection of claim 1 in view of Walton '494, the Office Action points out that the teachings of Walton '042 are incorporated by reference (see middle paragraph on page 3 of the Office Action). Applicant agrees.

However, the Office Action then contends that all transactions between a director and cache memory occur over a point-to-point connection in Walton '494 (see last paragraph on page 3, of the Office Action). To substantiate this contention, the Office Action further contends the controllers 20, 22 in Walton '042 are equivalent to the directors 122_0-122_7 in Walton '494, and that the directors/controllers in Walton '494 connect to cache memory 120 over a point-to-point connection (again, see last paragraph on page 3, of the Office Action). Applicant respectfully disagrees with this reasoning. There is no teaching in Walton '494 that a command passes over a point-to-point connection between a director/controller 122 and cache memory 120. Rather, as mentioned above in connection with Walton '494, the directors 122_0-122_7 further connect with the cache memory section 120 through bus A, bus B, bus C and bus D (see column 4, lines 23-25 and Fig. 2 of Walton '494) and ASICs A,A through D,D route information using signals on the busses A, B, C and D (see column 5, lines 41-44; column 6, lines 21-27 and Figs. 3 and 6 of Walton '494). Moreover, in connection with Walton '042, the controllers 20, 22 send commands through buses 28 as well. In particular, the controllers 20, 22 are adapted to assert commands on a bus portion 28a such as a read or write operation request, and to produce data and clock pulses on the portion 28b (see column 6, lines 14-29 Walton '042). Accordingly, in both Walton '494 and Walton '042, commands pass through busses. Thus, claim 1 patentably distinguishes over both Walton '494 and Walton '042, and the rejection of claim 1 under 35 U.S.C. §102(e) in view of Walton '494 and Walton '042 should be withdrawn.

Because claims 2-10 depend from and further limit claim 1, claims 2-10 patentably distinguish over Walton '494 and Walton '042 for at least the same reasons.

In connection with Fujimoto, there is no teaching of a method having steps of providing a command to a volatile memory cache circuit through a point-to-point channel between an interface circuit and the volatile memory cache circuit, and moving a data element through the point-to-point channel in accordance with the command, as recited in claim 1. Rather, in Fujimoto, control signals (REQ, ACK, etc.) pass through separate control lines 213 and data passes through an access path 136 (see column 9, line 21 through column 11, line 26 of Fujimoto). Accordingly, if one were to argue that the signal REQ is a command (see the contention made on page 4, last paragraph of the Office Action) and that the access path 136 is a point-to-point channel, the signal REQ clearly passes through control lines 213 and not the point-to-point channel as required by claim 1. As a result, claim 1 patentably distinguishes over Fujimoto, and the rejection of claim 1 under 35 U.S.C. §102(e) in view of Fujimoto should be withdrawn.

Because claims 2-10 depend from and further limit claim 1, claims 2-10 patentably distinguish over Fujimoto for at least the same reasons.

In connection with Steinmetz, there is no teaching of a point-to-point channel between an interface circuit and a volatile memory cache circuit, as recited in claim 1. Rather, Steinmetz discloses a disk array controller 200 having a cache memory 210 which connects to a first FC controller 206 through a first PCI bus 208, and connects to more FC controllers 216A-216N through a second PCI bus 214 which interface to a mass storage system 204 (see column 9, lines 1-8 and Fig. 6 of Steinmetz).

It should be understood that the Office Action contends that the Steinmetz high-speed serial FC data stream 188 is a point-to-point channel (see page 5, last paragraph of the Office Action). However, Applicant wishes to respectfully point out that the Steinmetz high-speed serial FC data stream 188 connects a host bus adaptor 182 to a number of peripheral devices 186 (see column 8, lines 45-54 and Figs. 4 and 5 of Steinmetz). Steinmetz does not disclose that the high-speed serial FC data stream 188 connects an interface circuit and a volatile

memory cache circuit, as recited in claim 1. Accordingly, claim 1 patentably distinguishes over Steinmetz, and the rejection of claim 1 under 35 U.S.C. §102(e) in view of Steinmetz should be withdrawn.

Because claims 2-10 depend from and further limit claim 1, claims 2-10 patentably distinguish over Steinmetz for at least the same reasons.

For the reasons stated above, claims 1-10 patentably distinguish over the cited references, and are in allowable condition.

Claims 11-20

Claim 11 is directed to a method for exchanging data with an interface circuit. The method is performed in a volatile memory cache circuit of a data storage system. The method includes the steps of receiving a command from the interface circuit through a point-to-point channel between the interface circuit and the volatile memory cache circuit, moving a data element through the point-to-point channel in accordance with the command, and providing status to the interface circuit through the point-to-point channel in accordance with the data element.

Applicant wishes to respectfully point out that arguments traversing the prior art rejection of claim 1 were presented above, and that similar arguments apply to claim 11. That is, claim 11 patentably distinguishes over Walton '494 (and Walton '042), Fujimoto and Steinmetz for reasons similar to those provided above in connection with claim 1. Accordingly, the rejections of claim 11 under 35 U.S.C. §102(e) should be withdrawn and claim 11 is in allowable condition.

Because claims 12-20 depend from and further limit claim 11 claims 12-20 patentably distinguish over the cited references for at least the same reasons.

Claims 21-29

Claim 21 is directed to a data storage system which includes a volatile memory cache circuit that buffers data elements exchanged between a storage device and a host, and an interface circuit that operates as an interface between

the volatile memory cache circuit and at least one of the storage device and the host. The data storage system further includes a point-to-point channel interconnected between the volatile memory cache circuit to the interface circuit. The point-to-point channel carries the data elements between the volatile memory cache circuit and the interface circuit.

Again, Applicant wishes to respectfully point out that arguments traversing the prior art rejection of claim were presented above, and that similar arguments apply to claim 11. That is, claim 21 patentably distinguishes over Walton '494 (and Walton '042), Fujimoto and Steinmetz for reasons similar to those provided above in connection with claim 1. Accordingly, the rejections of claim 21 under 35 U.S.C. §102(e) should be withdrawn and claim 21 is in allowable condition.

Because claims 22-29 depend from and further limit claim 21 claims 22-29 patentably distinguish over the cited references for at least the same reasons.

Claims 30-31

Claim 30 is directed to an interface circuit for a data storage system. The interface includes (i) a first adaptor that couples to at least one of a storage device and a host, (ii) a second adaptor that couples to a point-to-point channel leading to a volatile memory cache circuit which is capable of buffering data elements exchanged between the storage device and the host, and (iii) a controller coupled to the first adaptor and the second adaptor. The controller is configured to (i) provide a command to the volatile memory cache circuit through the point-to-point channel, (ii) move a data element between the interface circuit and the volatile memory cache circuit through the point-to-point channel in accordance with the command, and (iii) receive a status message from the volatile memory cache circuit through the point-to-point channel in accordance with the data element.

Similarly, claim 31 is directed to a volatile memory cache circuit for a data storage system. The volatile memory cache circuit includes an adaptor that couples to a point-to-point channel leading to an interface circuit which operates

as an interface between the volatile memory cache circuit and at least one of a storage device and a host, memory locations that are capable of buffering data elements exchanged between the storage device and the host, and a controller coupled to the adaptor and the memory locations. The controller is configured to (i) receive a command from the interface circuit through the point-to-point channel, (ii) move a data element between the volatile memory cache circuit and the interface circuit through the point-to-point channel in accordance with the command, and (iii) provide a status message to the interface circuit through the point-to-point channel in accordance with the data element.

Arguments similar to those set forth in traversing the prior art rejections of claim 1 apply to claims 30 and 31. That is, claims 30 and 31 patentably distinguishes over Walton '494 (and Walton '042), Fujimoto and Steinmetz for reasons similar to those provided above in connection with claim 1. Therefore, the rejections of claims 30 and 31 under 35 U.S.C. §102(e) should be withdrawn and claims 30 and 31 are in allowable condition.

Newly Added Claims

Claims 32-42 have been added and are believed to be in allowable condition. Claims 32-35 depend from claim 1. Claims 36-38 depend from claim 11. Claim 39-40 depend from claim 21. Claim 41 depends from claim 30. Claim 42 depends from claim 31. Support for claims 32-33, 36-37, 39 and 41-42 is provided within the Specification, for example, on page 15, line 26 through page 16, line 13 and Fig. 4. Support for claims 34-35, 38 and 40 is provided within the Specification, for example, on page 17, lines 4-26. No new matter has been added.

Conclusion

In view of the foregoing remarks, this Application should be in condition for allowance. A Notice to this affect is respectfully requested. If the Examiner believes, after this Amendment, that the Application is not in condition for allowance, the Examiner is respectfully requested to call the Applicant's Representative at the number below.

Applicant hereby petitions for any extension of time which is required to maintain the pendency of this case. If there is a fee occasioned by this Amendment, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 50-0901.

If the enclosed papers or fees are considered incomplete, the Patent Office is respectfully requested to contact the undersigned collect at (508) 366-9600, in Westborough, Massachusetts.

Respectfully submitted,

David E. Huang, Esq.
Attorney for Applicant
Registration No.: 39,229
CHAPIN & HUANG, L.L.C.
Westborough Office Park
1700 West Park Drive
Westborough, Massachusetts 01581
Telephone: (508) 366-9600
Facsimile: (508) 616-9805

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